IN THE CLAIMS

1 - 19. (CANCEL)

20. (ORIGINAL) A method for fabricating a semiconductor device with a plurality of field-effect transistors comprising:

forming a first device region, selected from the group consisting of a source region and a drain region, of a first field-effect transistor on a semiconductor layer;

forming a second device region, selected from the group consisting of a source region and a drain region, of a second field-effect transistor on said semiconductor layer;

forming a gate for said first field-effect transistor, wherein said gate has a first predetermined gate oxide thickness; and

forming a gate for said second field-effect transistor, wherein said gate has a second predetermined gate oxide thickness.

21. (ORIGINAL) The method of claim 20 including the additional step of configuring the first and the second device regions, and the first and the second gate regions into a circuit comprising two MOSFETs.

22. (ORIGINAL) The method of claim 20 wherein the step of forming the gate having the first predetermined gate oxide thickness and the step of forming the gate having the second predetermined gate oxide thickness, comprises:

forming a gate for the first field-effect transistor, wherein said gate has a first predetermined gate oxide thickness;

forming a gate for the second field-effect transistor, wherein said gate has a first predetermined gate oxide thickness;

removing the oxide from said gate of the first field-effect transistor;

forming gate oxide material on said gate for said first field-effect transistor;

forming gate oxide material on said gate for said second field-effect transistor; and

such that the gate oxide of the first field-effect transistor has a thickness less than the thickness of the gate oxide for the second field-effect transistor.

23. (ORIGINAL) The method of claim 20 wherein the first and the second field-effects transistors can withstand different gate input voltages as a consequence of the differing predetermined gate oxide thickness.

24. (ORIGINAL) A method for fabricating a semiconductor device with a plurality of transistors comprising:

forming first and second spaced-apart diffusion regions on a semiconductor layer;

forming a third semiconductor region over said first diffusion region, wherein said third semiconductor region has an opposite conductivity type than said first diffusion region;

forming a fourth semiconductor region over said second diffusion region wherein said fourth semiconductor region has an opposite conductivity type than said second diffusion region;

forming a first gate oxide of a first predetermined thickness adjacent said third semiconductor region;

forming a second gate oxide of a second predetermined thickness adjacent said fourth semiconductor region;

forming fifth and sixth semiconductor regions, each positioned over one of said third and said fourth semiconductor regions, such that said third and said fifth regions are vertically aligned with one of said first and said second regions, and such that said fourth and said sixth regions are vertically aligned with the other of said first and second regions, the resulting structure providing two transistors.

25. (ORIGINAL) The method of claim 24 wherein the step of forming the first gate oxide of a first predetermined thickness adjacent the third semiconductor region and the step of forming the second gate oxide of the second predetermined thickness adjacent the fourth semiconductor region comprises:

forming a first gate oxide of a first predetermined thickness adjacent said third semiconductor region;

forming a second gate oxide of said first predetermined thickness adjacent said fourth semiconductor region;

removing said first gate oxide;

forming a third gate oxide of a second predetermined thickness adjacent said third semiconductor region;

forming said third gate oxide of said third predetermined thickness adjacent said fourth semiconductor region; and

wherein the gate oxide thickness adjacent said fourth semiconductor region is the sum of said first predetermined thickness plus said second predetermined thickness.

26. (ORIGINAL) The method of claim 24 wherein the first and the second gate oxides are associated with a first and a second MOSFET, and wherein said first and said second MOSFETs form a complimentary MOSFET device, and wherein said third and said fourth gates are associated with a third and a fourth MOSFET, respectively, and wherein said third and said fourth MOSFETs form a second complimentary MOSFET device; and wherein the gate terminals of said first complimentary MOSFET device have a first breakdown voltage related to the first predetermined thickness, and wherein the gate terminals of said second MOSFET device have a second breakdown voltage related to the second predetermined thickness.